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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,803	01/26/2004	Payman Zarkesh-Ha	02-5938	9749

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EXAMINER	
KIM, SU C	
ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
02/04/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/764,803	ZARKESH-HA ET AL.	
	Examiner	Art Unit	
	SU C. KIM	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/25/2008 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 7-13, 15-17, & 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Voogel (US 6,362,651) in view of Muthujumaraswathy et al. (US 6,279,045).

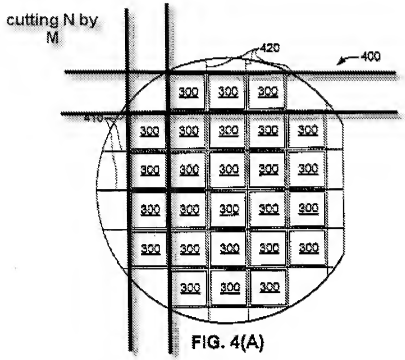

FIG. 4(A)

Regarding claims 1, 9, & 17, Voogle discloses a method for providing field programmable platform array units, comprising:

cutting N by M array of platform array units 300 (Fig. 4(A)) within a single platform array unit platform 300 from a field programmable platform array wafer 400 according to an order for a customer, N and M being positive integers, said field programmable platform array wafer 300 having all silicon layers and metal layers already built (Col. 2, lines 65-67, Col. 3 lines1-3) and including a plurality of platform array units (col. 1, 19-39, note: programmable logic device (PLDS)) said plurality of platform array units having portions being field programmable by a customer (note: by user) and interconnect 610 between said plurality of platform array units 450(1) & 450(2) being pre-routed on chip (Fig. 6); and packaging and testing (Col.6, lines 59-65) said N by M array of platform array units.

Voogle fails to teach each of said plurality of platform array units including at least one core and at least one processor.

However, Muthujumaraswathy disclose a chip including at least one core and at least one processor (Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to provide each of said plurality of platform array units including at least one core and at least one processor, Voogle with each of said plurality of platform array units including at least one core and at least one processor as taught by Muthujumaraswathy in order to provide power or process saving (Col. 5, lines 1-3).

Regarding claims 2 & 10, as applied to claims 1 & 9, Voogle and Muthujumaraswathy in combinations disclose that programming said N by M array of platform array units by said customer (note: all the FPGA are produced for the customer).

Regarding claims 3 & 11, as applied to claims 12 & 10, Voogle and Muthujumaraswathy in combinations disclose that said programming is performed for at least one of unit specialization, unit role assignment, and inter-unit communications (Muthujumaraswathy, Fig. 2(A)).

Regarding claims 4, 12 & 24, as applied to claims 2, 10, & 17, Voogle and Muthujumaraswathy in combinations disclose that said programming is performed with firmware (Voogle, col. 1 lines 18-26).

Regarding claims 5 & 13, as applied to claims 1 & 9, Voogle and Muthujumaraswathy in combinations disclose that said N by M array of platform array units are within a single platform (Muthujumaraswathy, Fig. 2, note: a single platform 100).

Regarding claims 7 & 15, as applied to claims 5 & 13, Voogle and Muthujumaraswathy in combinations disclose said single platform is a digital signal processing (DSP) platform (Muthujumaraswathy, col. 3, line 62 note: a processor).

Regarding claims 8 & 16, as applied to claims 1& 9, Voogle and Muthujumaraswathy in combination discloses that storing said field programmable platform array wafer (Voogle, col. 1 lines 18-26).

4. Claims 6 & 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Voogel (US 6,362,651) in view of Muthujumaraswathy et al. (US 6,279,045) and further in view of Mastro et al. (US 2002/0091977).

Regarding claims 6 & 14, as applied to claims 5 & 13, Voogle and Muthujumaraswathy in combinations discloses that said single platform

Voogle and Muthujumaraswathy in combinations fail to teach said single platform is a storage area network (SAN) platform.

However, Mastro suggests said single platform 94 (Fig. 5, FPGA) is a storage area network (paragraph 0067).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Voogle and

Muthujumaraswathy in combination with said single platform is a storage area network (SAN) platform as taught by Mastro in order to enhance functionality.

5. Claims 18 & 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Voogel (US 6,362,651) in view of Muthujumaraswathy et al. (US 6,279,045) and further in view of Lee et al. (US 6,222,212).

Regarding claims 18 & 20-23, Voogle and Muthujumaraswathy in combinations disclose that said semiconductor device includes top pad and said top pad 456 of said semiconductor device are used as a routing layer for the pre-touted interconnect 610 between said plurality of platform array units (Voogle, Fig. 6).

Voogle and Muthujumaraswathy in combinations fails to teach top pad are aluminum, metal bumps, copper, polysilicon, or silicon layer.

However, Lee discloses that interconnection (routing layer) can be made of aluminum, copper, polycrystalline silicon, or metal bumps 908 (Col. 5, lines 30-61, Fig. 9B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Voogle and Muthujumaraswathy in combinations with interconnection (routing layer) can be made of aluminum, copper, polycrystalline silicon as taught by Lee in order to enhance electrical conductivity.

6. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over by Voogel (US 6,362,651) in view of Muthujumaraswathy et al. (US 6,279,045) and further in view of Hung et al. (US 6,396,129).

Regarding claim 19, as applied to claim 18, Voogle and Muthujumaraswathy in combinations disclose that said semiconductor device.

Voogle and Muthujumaraswathy in combinations fail to teach encapsulation of lower metal layers of said semiconductor device.

However, Huang discloses encapsulation 150 of lower copper layer (Fig. 3C, col. 4, lines 20-43).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Voogle and Muthujumaraswathy in combinations with encapsulation of lower copper layer as taught by Haung in order to enhance bonding strength.

Response to Arguments

7. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SU C. KIM whose telephone number is (571)272-5972. The examiner can normally be reached on Monday - Friday, 10:00AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SU C KIM/
Examiner, Art Unit 2823

/W. David Coleman/
Primary Examiner, Art Unit 2823